JEDEC STANDARD

Bus Interconnect Logic (BIC) for 1.2 Volts

JESD8-16A

(Revision of JESD8-16)

NOVEMBER 2004

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2004
2500 Wilson Boulevard
Arlington, VA 22201-3834

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications online at
http://www.jedec.org/Catalog/catalog.cfm

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V

(From JEDEC Board Ballot JCB-04-101, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input and output specifications for devices that are designed to operate in the BIC logic switching range, nominally 0 V to 1.2 V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages; however, the V_{DD} value is not specified in this standard. The standard also suggests bus configurations in which optimum performance may be gained.

The standard defines the voltage thresholds, termination schemes, and test conditions for BIC compatibility. Class structures have been established to standardize output drive characteristics under various application conditions. Vendors may specify tighter tolerances on any or all parameters to increase performance.

2 Overview

BIC is defined in both a differential form and a single ended with V_{REF} form. While the two versions have different signal requirements and are not fully interchangeable, they are compatible at the signal level and can be interconnected with minimal performance degradation.

BIC is optimized for use with on die termination (ODT). In some applications, this allows the components on the interface to be actively tuned for optimum performance and low noise under varying conditions.

The single ended version has been optimized for parallel bus operation, requiring termination at both the source and receiver. It is expected that all termination will be on die, eliminating the need for external resistors, but external resistive components are compatible with BIC should the application require them.

The differential version of BIC has been optimized for distributing clock signals or other very high-speed signals where signal integrity is critical. Differential BIC can also be used for parallel busses, if the user can tolerate the extra signal lines required for differential signaling.

This standard is a physical interface only and does not define training, or other potential bus architecture requirements, but BIC is fully compatible with these if the user wishes to expand upon BIC capabilities.

3 Standard specifications for single ended interfaces

3.1 Supply voltage levels

Table 1 — Supply voltage levels

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Device supply voltage	n/a	n/a	n/a	V	1
V_{DDQ}	Output supply voltage	1.14	1.2	1.26	V	
V_{REF}(dc)	Input reference voltage	0.48 * V_{DDQ}	0.5 * V_{DDQ}	0.52 * V_{DDQ}	V	2
V_{REF}(ac)	Input reference voltage	0.47 * V_{DDQ}	0.5 * V_{DDQ}	0.53 * V_{DDQ}	V	2
V_{TT}	Termination voltage		V_{DDQ}/2		V	3

NOTE 1 Interface is not affected by device core voltage.

NOTE 2 The referenced V_{DDQ} is the power supply voltage for the device receiving the V_{REF} input. V_{REF}(ac) is V_{REF}(dc) plus noise. Peak to peak noise on V_{REF}(ac) may not exceed 2% of V_{REF}(dc).

NOTE 3 The interface may be used with either ODT or external termination. The termination voltage V_{TT} may either be supplied by an independent power supply or created through a Thevenin equivalent circuit. Regardless, the termination should be arranged for optimum signal integrity balanced at V_{DDQ}/2 at the receiver. The min and max values should be set by the system designer to meet application needs.

3.2 Input voltage levels

Table 2 — Input voltage levels

Symbol	Parameter	Min.	Nom	Max	Units	Notes
V_{IH}(dc)	dc input high	V_{REF} + 0.08		V_{DDQ} + 0.15	V	4, 6
V_{IL}(dc)	dc input low	-0.15		V_{REF} - 0.08	V	6
V_{IH}(ac)	ac input high	V_{REF} + 0.15		V_{DDQ} + 0.24	V	4, 5, 6
V_{IL}(ac)	ac input low	-0.24		V_{REF} - 0.15	V	5, 6

NOTE 4 It is expected that most BIC compatible devices will utilize input clamp diodes, restricting the input voltage to the levels shown. For devices that have been specifically designed for hot insertion or power down on an active bus, the maximum input voltage shall be 1.26 V, regardless of the level of V_{DDQ}.

NOTE 5 The ac timing measurements, including propagation delays and setup/hold times will be measured beginning when the input signal crosses V_{REF}. The ac overshoot above V_{DDQ} and below V_{SS} should not exceed 20% of the duty cycle of the signal, or exceed vendor specified limits.

NOTE 6 For optimum noise margin and performance, the signal must maintain a center balance around V_{DDQ}/2, V_{REF}, and $V_{TT,}$ both at the driver and the receiver. Furthermore, V_{REF} of the receiving device should track the variations in the dc value of the V_{DDQ} of the sending device.

3 Standard specifications for single ended interfaces (cont'd)

3.3 Devices with On Die Termination (ODT)

The standard termination for BIC is a resistor (R_T) at the end of the transmission line tied to a voltage level (V_T) that is ½ V_{DDQ}. BIC devices may perform the termination function internally with On Die Termination (ODT) or externally with discrete devices. V_T may be externally supplied, internally supplied, or generated through a Thevenin equivalent circuit within the device. If ODT is used, the parameters for specifying ODT as shown in Table 3 must be used.

Table 3 — BIC Input Impedance Parameters for Devices with Thevenin ODT

Symbol	Parameter Description	Units	Notes
R_T	Termination impedance	Ω	7
R_{IL}	Specified input impedance when the input is logic low	Ω	8
R_{IH}	Specified input impedance when the input is logic high	Ω	9
$R_I\Delta$	Correlation between R_{IL} and R_{IH}	%	10

NOTE 7 R_T is the termination impedance. In order to identify differences in the value of R_T between input high and low conditions in ODT devices, the value of R_T will be described and specified as R_{IL} when the input is low and R_{IH} when the input is high. Either R_T or both R_{IL} and R_{IH} must be specified. It is not necessary to specify all three values.

NOTE 8 R_{IL} is the value of R_T when ODT is active and the input is held at the nominal logic low position. The tested value of R_{IL} must not exceed ±15% of the specified value of R_{IL}.

NOTE 9 R_{IH} is the value of R_T when ODT is active and the input is held at the nominal logic high position. The tested value of R_{IH} must not exceed ±15% of the specified value of R_{IH}.

NOTE 10 $R_I\Delta$ = (actual R_{IH} – actual R_{IL}) / (0.5 * (actual R_{IH} + actual R_{IL})). The correlation between R_{IL} and R_{IH} must not exceed 10%.

3.3.1 Testing devices with On Die Termination (ODT)

The testing of ODT consists of forcing a current, and verifying that the input voltage falls within an expected range. This test is performed at the nominal logic high and low voltage levels. If the values of either R_T or V_T are outside of tolerances, one or both of the tests will fail. Table 4 shows the test condition limits for a BIC input with ODT turned on with ±15% impedance tolerance. The measured values of V_{IL} and V_{IH} must be used to calculate and guarantee $R_I\Delta$.

Table 4 — Impedance test Limits

Symbol	Parameter and Condition	Min	Nom	Max	Unit
V_{IL}	Input low, I_{IL} = 0.25 * V_{DDQ} / R_{IL}	0.212 * V_{DDQ}	0.25 * V_{DDQ}	0.288 * V_{DDQ}	V
V_{IH}	Input high, I_{IH} = -0.25 * V_{DDQ} / R_{IH}	0.712 * V_{DDQ}	0.75 * V_{DDQ}	0.788 * V_{DDQ}	V

3.3 Devices with On Die Termination (ODT) (cont'd)

3.3.2 Applications information for ODT use with BIC (for reference only)

When optimizing ODT for use in typical transmission line environments, the ODT impedance should be equal to or greater than the transmission line impedance for optimal performance. Setting the ODT impedance to match the transmission line impedance will avoid reflections in ideal applications. In less than ideal applications, losses, noise and other anomalies will degrade the signal on the transmission line prior to the arrival at the ODT, making it desirable to slightly increase the impedance value of ODT to compensate. Increasing the value of ODT impedance will increase the edge rate of incoming signals in most applications, benefiting timing margins and accuracy.

Implementation of ODT as a Thevenin circuit to V_{DDQ} increases power dissipation by providing a current path directly through the pull up and pull down impedances from V_{DDQ} to V_{SS}. Increasing the ODT impedance of Thevenin implementations will reduce power consumption. Turning ODT off when the device is not receiving will also reduce power consumption in Thevenin implementations. This is especially true in bi-directional devices when the device is transmitting.

Table 5 shows an example of an ODT specification for use in a 50 Ω environment. In the example, the impedance is specified as both an R_{IL} and R_{IH}. The impedance is set at 55 Ω to allow for losses and to provide a clean signal edge. In addition, the vendor would need to include a table similar to Table 4 to guarantee test limits.

Table 5 — Example of an ODT specification for a 50 W environment

Symbol	Parameter Description	Value	Units
R_T	Termination impedance	55	Ω
$R_I\Delta^{\dagger}$	Correlation between R_{IL} and R_{IH}	±10	%

† $R_I\Delta = (R_{IH} - R_{IL}) / (0.5 * (R_{IH} + R_{IL}))$ where R_{IH} is R_T measured at $V_I = 0.75 * V_{DDQ}$ and R_{IL} is R_T measured at $V_I = 0.25 * V_{DDQ}$.

Table 6 shows an example of an ODT specification for a device with adjustable input impedance. In the example, the impedance can be set at any value from 55 Ω to 85 Ω. The vendor would also need to include a table similar to Table 4 to guarantee test limits.

Table 6 — Example of a specification for a device with variable ODT

Symbol	Parameter Description	Min	Max	Units
R_{IL}	Specified input impedance when the input is logic low	50	85	Ω
R_{IH}	Specified input impedance when the input is logic high	50	85	Ω
$R_I\Delta^{\dagger}$	Correlation between R_{IL} and R_{IH}		±10	%

† $R_I\Delta = (R_{IH} - R_{IL}) / (0.5 * (R_{IH} + R_{IL}))$ where R_{IH} measured at $V_I = 0.75 * V_{DDQ}$ and R_{IL} is measured at $V_I = 0.25 * V_{DDQ}$.

3 Standard specifications for single ended interfaces (cont'd)

3.4 Output characteristics

It is intended that BIC outputs will be standard CMOS outputs with fairly linear impedance curves as shown in the VI diagrams in Figure 1. The left figure shows the desired pull down characteristics (R_{OL}) and the right figure shows the desired pull up characteristics (R_{OH}). Testing of R_{OL} and R_{OH} would be performed by forcing I_{OL} and I_{OH}, then verifying that V_{OL} and V_{OH} fall within the test limits as shown in Figures 1 and 2. The gray areas are the valid ranges for R_{OL} and R_{OH}. Current flowing into a device is considered positive current. Current flowing out of a device is considered negative current. Therefore, I_{OL} is described as a positive value and I_{OH} is described as a negative value.

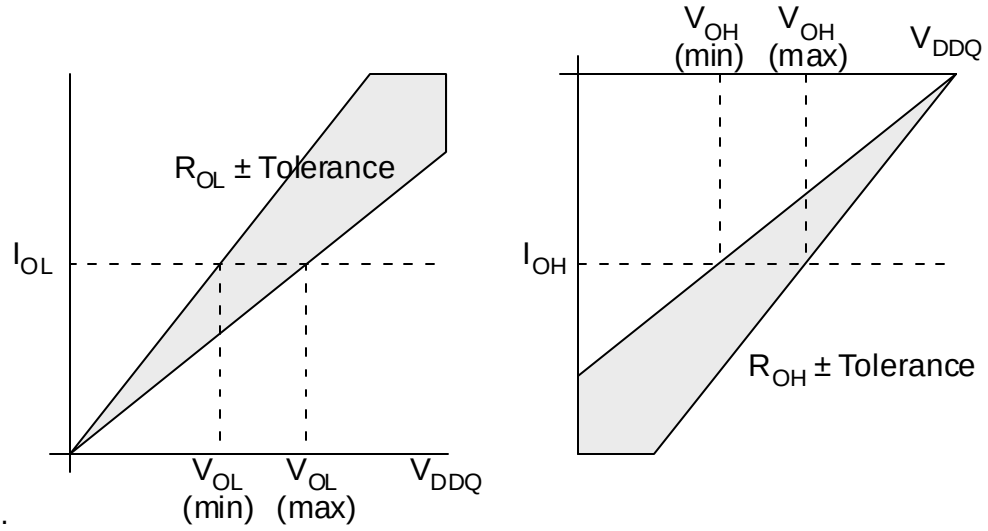


Figure 1 — Idealized V/I curves for V_{OL} and V_{OH} measurements

Most BIC outputs will limit output voltage to the values shown in Table 7. For devices that have been specifically designed for hot insertion into a powered system or power down on an active bus, the maximum output voltage shall be 1.26V, regardless of the level of V_{DDQ}. The undefined values in Table 7 are characteristic of the device output impedance and are defined by the class type in the following section.

Table 7 — Output voltage levels

Symbol	Parameter	Min.	Nom	Max	Units	Notes
V_{OH}(dc)	Output high voltage			V_{DDQ} + 0.15	V	11
V_{OL}(dc)	Output low voltage	-0.15			V	
V_{OH}(ac)	Output high voltage			V_{DDQ} + 0.24	V	11, 12
V_{OL}(ac)	Output low voltage	-0.24			V	12

NOTE 11 Devices that have been designed for hot insertion or power down in an active system may allow voltages in excess of the maximum value.

NOTE 12 The total ac overshoot above V_{DDQ} and below V_{SS} should not exceed 20% of the duty cycle of the signal, or exceed vendor specified limits.

3.4 Output characteristics (cont'd)

3.4.1 Output drive specifications

BIC output drivers are defined in terms of the output impedance of the drivers and a tolerance on the output impedance. The maximum tolerance window on output impedance for BIC compliance has been set at ±15% of the specified impedance. Tighter tolerances may be specified by the vendor. Table 8 lists the three distinguishing parameters that define a BIC output class. These are the pull up impedance, the pull down impedance, and the tolerance between the two.

Table 8 — BIC output impedance parameters

Symbol	Parameter Description	Units	Notes
R_{OL}	Specified output impedance when driving a logic low	Ω	
R_{OH}	Specified output impedance when driving a logic high	Ω	
RΔ	Correlation between R_{OL} and R_{OH}	%	13

NOTE 13 RΔ = (actual R_{OH} – actual R_{OL}) / (0.5 * (actual R_{OH} + actual R_{OL})).

Device compliance testing will be completed primarily at the characterization level, with test limits verified at the operating limits of voltage and temperature. If the outputs have variable impedance, the testing will be performed over the entire specified impedance range. Production testing will be required only under representative conditions and impedance levels with all other conditions guaranteed by correlation.

3.4.2 Impedance test limits

Using ohm's law with the specified impedance, the expected currents when driving V_{OL} and V_{OH} can be calculated. During testing, the calculated current will be forced, and the actual V_{OH} or V_{OL} verified to fall within limits. In order to verify a reasonable monotonicity to the VI curve, two test points must be verified during characterization testing, but only one of the two is required for production testing.

The specified values for V_{OH} are 0.5 * V_{DDQ} and 0.75 * V_{DDQ}. The specified values for V_{OL} are 0.5 * V_{DDQ} and 0.25 * V_{DDQ}. The driving currents at these voltages must be calculated and used for testing as shown in Figure 2. The tolerance of the actual V_{OH} and V_{OL} is verified as shown in Figure 1. The value of RΔ is calculated from the test values and must not exceed ±10% for BIC compliance.

3.4 Output characteristics (cont'd)

3.4.2 Impedance test limits (cont'd)

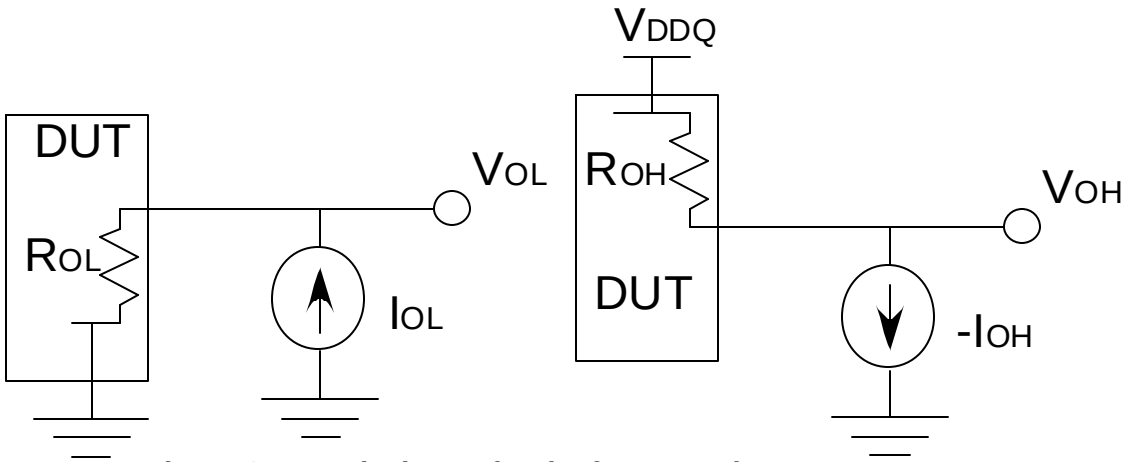


Figure 2 — Typical test circuits for V_{OL} and V_{OH} measurements

The test limits for BIC compliance for all classes are shown in Table 9 with the primary test point at 0.5 * V_{DDQ} for V_{OH} and V_{OL}. The values shown limit the tolerance on R_{OH} and R_{OL} to ±15% of the specified value at the voltage midpoint, which is the maximum tolerance allowed for BIC compliance. Tighter tolerances may be specified by the vendor. As an example, using a range of 0.45 * V_{DDQ} to 0.55 * V_{DDQ} would provide an output impedance tolerance of ±10% at 0.5 * V_{DDQ}. In addition to the impedance test at the midpoint, a second test is taken at 0.25 * V_{DDQ} for V_{OL} and 0.75 * V_{DDQ} for V_{OH}. These secondary test points insure driving capability at the typical dc logic high and low in a typical system with well-balanced termination.

Table 9 — Impedance test limits

Sym	Parameter and Condition	Min.	Nom	Max	Units
V_{OH}	Output high, I_{OH} = -0.5 * V_{DDQ} / R_{OH}	0.425 * V_{DDQ}	0.5 * V_{DDQ}	0.575 * V_{DDQ}	V
V_{OH}	Output high, I_{OH} = -0.25 * V_{DDQ} / R_{OH}	0.712 * V_{DDQ}	0.75 * V_{DDQ}	--	V
V_{OL}	Output low, I_{OL} = 0.5 * V_{DDQ} / R_{OL}	0.425 * V_{DDQ}	0.5 * V_{DDQ}	0.575 * V_{DDQ}	V
V_{OL}	Output low, I_{OL} = 0.25 * V_{DDQ} / R_{OL}	--	0.25 * V_{DDQ}	0.288 * V_{DDQ}	V

3 Standard specifications for single ended interfaces (cont'd)

3.5 Output classes

BIC has three defined output classes. BIC Class 1 (BIC1) has been optimized for driving 50 Ω environments or transmission lines. BIC Class 2 (BIC2) has been optimized for driving 25 Ω environments (e.g. a 50 Ω transmission line with a 50 Ω termination at both ends). BIC Class 3 (BIC3) allows a user to adjust the device output impedance between 40 Ω and 50 Ω or a larger vendor specified range. These classes have been defined to assist in defining components for the described applications. All BIC components must fully comply with sections 3.4, 3.4.1 and 3.4.2. It is not necessary to declare compatibility to an output class to claim compatibility with the BIC Standard.

3.5.1 BIC1 – BIC Class 1 with fixed impedance output

BIC Class 1 output buffers are intended for symmetrically parallel terminated load environments, with equivalent termination resistance R_T to termination voltage V_{TT}. The nominal impedance of 44 Ω has been selected to optimally drive a 50 Ω environment.

Table 10 — BIC1 Output Impedance Parameters

Symbol	Parameter Description	Nominal	Unit
R_{OL}	Specified output impedance when driving a logic low	44	Ω
R_{OH}	Specified output impedance when driving a logic high	44	Ω
RΔ	Correlation between R_{OL} and R_{OH}	±10	%

3.5.1.1 Applications information BIC Class 1 interfaces (for reference only)

Figure 3 shows a possible usage of BIC1 in a unidirectional application. The termination resistor R_T may be either an "on die" termination or an external resistor. The source impedance of BIC1 is approximately 44 Ω, and is intended for use in a point-to-point application. The value of R_T should be set to provide optimum signal integrity at the receiver.

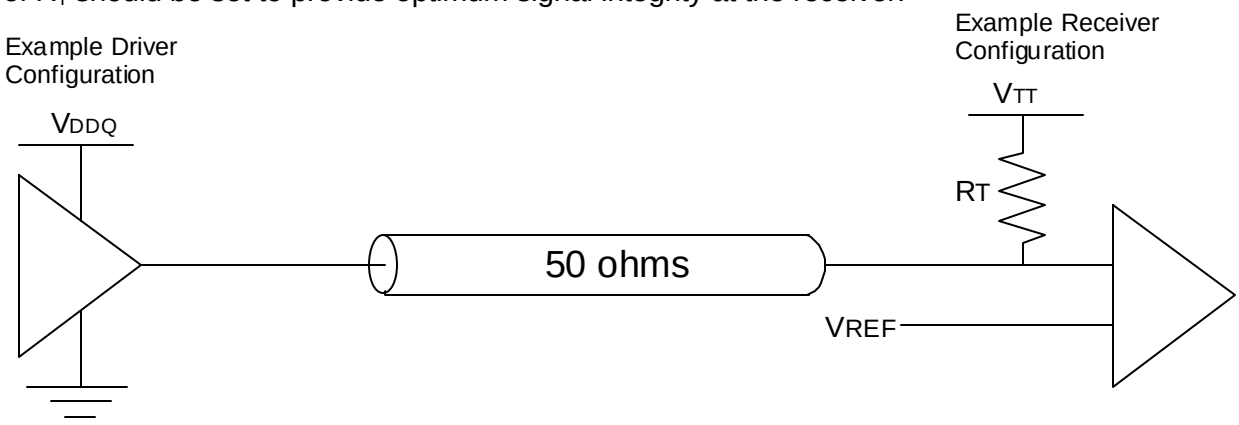


Figure 3 — Example of BIC Class 1 usage

3.5 Output classes

3.5.2 BIC2 – BIC Class 2 with Fixed Impedance Output

BIC Class 2 output buffers are intended for symmetrically double parallel terminated load environments, with equivalent termination resistance R_{T1} and R_{T2} each to termination voltage V_{TT}.

Table 11 — BIC2 Output Impedance Parameters

Symbol	Parameter Description	Nominal	Unit
R_{OL}	Specified output impedance when driving a logic low	22	Ω
R_{OH}	Specified output impedance when driving a logic high	22	Ω
RΔ	Correlation between R_{OL} and R_{OH}	±10	%

3.5.2.1 Applications information for BIC Class 2 interfaces (for reference only)

Figure 4 shows a possible usage of BIC2 in a bi-directional application. The termination resistors R_T may be either "on die" termination or external resistors. The approximately 22Ω source impedance of BIC2 drivers has been set to drive the parallel impedances of the transmission line and the termination resistor R_T at the near end. At the far end of the transmission line, the termination resistor should match the transmission line impedance, providing optimum signal integrity.

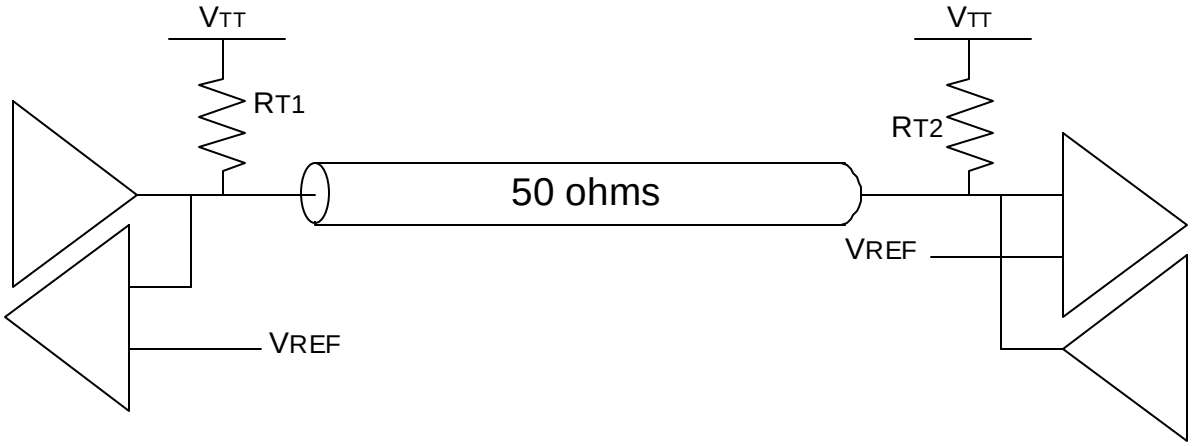


Figure 4 — Example of BIC Class 2 usage

In applications where the termination resistors R_T are "on die" it may be possible to disable the resistor at the driving end of the transmission line. Possible effects of this may be a reduction in power consumption, improved signal integrity if the transmission line is heavily loaded, and the ability to use BIC1 drivers.

In the event that the user wishes to create a multidrop application with a single driver driving several receivers, the user may disable the ODT on all receivers except those at the end(s) of the transmission line.

3.5 Output classes

3.5.3 BIC3 – BIC Class 3 with adjustable output impedance

BIC Class 3 is intended for devices that have the ability to adjust the impedance of their output drivers through a user-controlled mechanism. The adjustment may be achieved through digital programming, the use of an external resistor, or other means. The distinguishing characteristic of BIC3 is the adjustability of the impedance. It is possible that a user could adjust the output of a BIC Class 3 device to fully comply with BIC Class 1 specifications. Some BIC3 devices may have the ability to adjust the output impedance low enough to meet BIC2 specifications, but the ability to go lower than 40 Ω is not required.

The vendor must specify the adjustable range of the output impedance on BIC3 devices, and the tolerance between the programmed value and the actual value. More than one range may be specified for a device. For example, a device may have a narrow impedance range with a high correlation between the programmed value and the actual value, and a wider impedance range with relaxed correlation.

The vendor may specify any range for output impedance, but to claim compliance to BIC3, the range must include 40 Ω through 50 Ω and a tolerance not exceeding ±15%. An example of a BIC3 device specification with a range from 22 to 50Ω with a ±15% tolerance between the programmed output impedance and the actual output impedance is as shown in Table 12. A device of this type would be compliant to both BIC Class 1 and BIC Class 2.

Table 12 — BIC3 Example output impedance ranges

Sym	Parameter description	Min	Max	Tol.	Unit	Note
R_{OL}	Programmable impedance range for R_{OL}	22	50	±15%	Ω	14
R_{OH}	Programmable impedance range for R_{OH}	22	50	±15%	Ω	14
RΔ	Correlation between R_{OL} and R_{OH} over range		±10		%	15

NOTE 14 This parameter shows the minimum programmable impedance, the maximum programmable impedance and the tolerance with which the programmed value will match the actual value. The tolerance is calculated by subtracting the actual output impedance from the programmed impedance and then dividing by the programmed impedance value.

NOTE 15 RΔ = (actual R_{OH} – actual R_{OL}) / (0.5 * (actual R_{OH} + actual R_{OL})).

3.5.3 BIC3 – BIC Class 3 with adjustable output impedance (cont'd)

3.5.3.1 Applications information for BIC Class 3 (for reference only)

Figure 5 shows an example of a BIC3 adjustable impedance output, driving a single load in a point-to-point application utilizing external termination. Through the adjustment of Ro, BIC3 can be adapted for other applications, including bi-directional, multi-drop, and ODT.

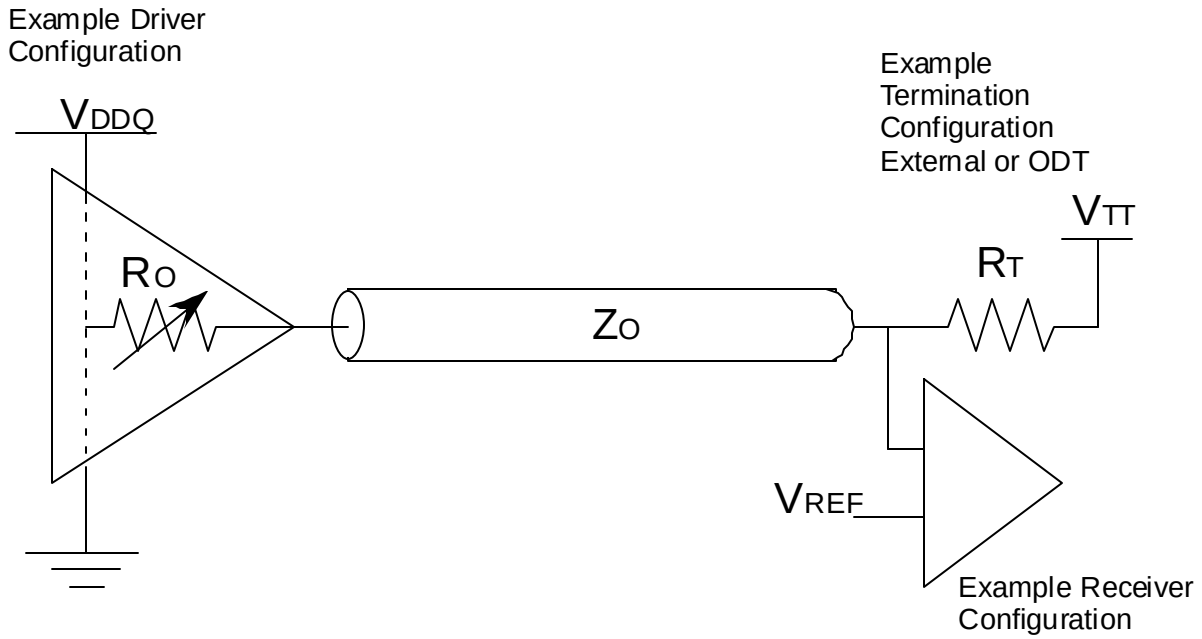


Figure 5 — Example of BIC Class 3 usage

3.6 Termination information for all classes (for reference only)

To maximize performance under nominal conditions, the following parameter restrictions should be observed. In applications where Z_O is lossy, cross coupling exists, or other circuit anomalies exist, it may be necessary to adjust R_T and V_{TT} beyond the limits shown to adapt to the application.

Table 13 — BIC termination guidelines

Symbol	Parameter	Min	Nominal	Max	Units	Note
R_T	Termination impedance	Z_O	1.10 * Z_O	1.20 * Z_O	Ω	16
V_{TT}	Termination voltage	0.47 * V_{DDQ}	0.5 * V_{DDQ}	0.53 * V_{DDQ}	V	17

NOTE 16 Z_O is the nominal impedance of the transmission line. The values shown are intended to optimally terminate a point-to-point unidirectional transmission line. In some applications where other concerns exist, such as power dissipation, and transmission line anomalies, it may be beneficial to use a value of R_T that is much higher than the maximum shown.

NOTE 17 The referenced V_{DDQ} is the power supply voltage for the receiver closest to the termination.

4 Standard specifications for differential interfaces

4.1 Supply voltage levels

Table 14 — Differential supply voltage levels

Symbol	Parameter	Min.	Nom	Max	Units	Notes
V_{DD}	Device supply voltage	n/a	n/a	n/a	V	1
V_{DDQ}	Output supply voltage	1.14	1.2	1.26	V	

NOTE 1 Interface is not affected by device core voltage

4.2 Input voltage levels

Table 15 — Differential input voltage levels

Symbol	Parameter	Min.	Nom	Max	Units	Notes
V_{IX}	Input voltage cross point		0.5 * V_{DDQ}		V	2
V_{DIF}(ac)	ac input differential voltage	0.30		V_{DDQ} + 0.48	V	3
V_{DIF}(dc)	dc input differential voltage	0.16		V_{DDQ} + 0.30	V	
V_{DIF}(cm)	dc common mode input	0.4 * V_{DDQ}	0.5 * V_{DDQ}	0.6 * V_{DDQ}	V	4
V_{IN}(ac)	ac input voltage	-0.24		V_{DDQ} + 0.24	V	5
V_{IN}(dc)	dc input voltage	-0.15		V_{DDQ} + 0.15	V	5

NOTE 2 V_{IX} is nominally 0.5 * V_{DDQ}. The minimum and maximum limits are set by the application.

NOTE 3 The trigger point for ac timing measurements, including propagation delays and setup/hold times will be the differential signal cross point (differential voltage = zero).

NOTE 4 The dc common mode input voltage must be maintained to guarantee timing parameters and switching levels. The user may specify a more restricted range, if the application requires it. Specifying an ac common mode input voltage is at the user's discretion.

NOTE 5 The allowable limit for the excursion of either differential input in devices that utilize input clamp diodes (most BIC devices). For devices that have been specifically designed for hot insertion or power down on an active bus, the maximum input voltage of either differential input shall be 1.26V, regardless of the level of V_{DDQ}.

4.3 Output voltage levels

Table 16 — Differential output voltage levels

Symbol	Parameter	Min.	Nom	Max	Units	Notes
V_{OX}	Output voltage cross point		0.5 * V_{DDQ}		V	6
V_{OH}(dif)	Output differential voltage				V	7
V_{OL}(dif)	Output differential voltage				V	7
V_{OUT}(ac)	ac output voltage	-0.24		V_{DDQ} + 0.24	V	8
V_{OUT}(dc)	dc output voltage	-0.15		V_{DDQ} + 0.15	V	8

NOTE 6 V_{OX} is nominally 0.5 * V_{DDQ}. The minimum and maximum limits are set by the application.

NOTE 7 Loading conditions must be specified in the data sheet and compatible with intended applications. The differential voltage is measured between the two differential outputs. All voltages for V_{OH} and V_{OL} are defined by the class type.

NOTE 8 The allowable limit for the excursion of either differential output. The ac overshoot above V_{DDQ} and below V_{SS} should not exceed 20% of the duty cycle of the signal, or exceed vendor specified limits.

4.4 Applications information for differential BIC interfaces (for reference only)

The differential specifications for BIC utilize both series and parallel termination resistors. It is expected that the resistors are “on die”, but in cases without ODT, external resistors can be used. It is also expected that the on die resistors will have an ability to adjust their impedance to optimize signal integrity and interface performance.

Figure 6 shows a possible usage of a BIC interface in a unidirectional differential application with on die adjustable resistors on both ends of the signal line. The termination at the receiver end is across the differential lines and has no connection to any termination voltage. The driver is a differential and has series termination in both polarities of the driver.

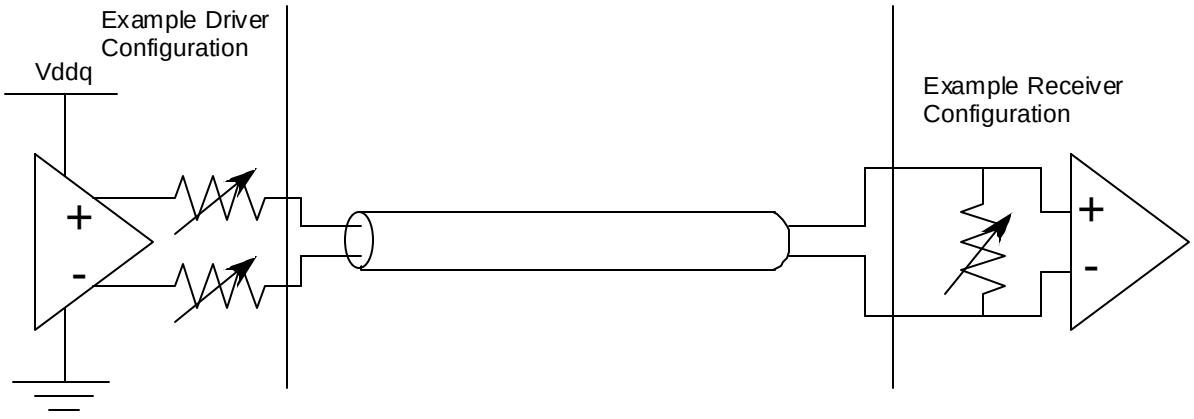


Figure 6 — Example of BIC in a differential application

Utilizing on die termination, the user may have the ability to actively reconfigure the termination scheme and reverse the signal flow in the line, creating a bi-directional bus.

5 Test circuits and waveforms

In order to provide uniform testing of device output enable and disable times, the following guidelines are given. The specific loading of the device outputs to create the voltage shifts shown must be specified in the device data sheet, but due to variation of device types and their characteristics, it is not possible to specify the specific load in this document.

For all devices the disable time is the time measured from the device receiving the disable input to the time the device indicates it has released the output by changing from a driven output to high impedance. Because there is no active driver on the line when the output is disabled, a small voltage shift caused by a load resistance connected to the opposite rail is sufficient to indicate the high impedance characteristic.

For all devices, the measurement of enable times is accomplished by measuring the time it takes for the device to transition from a disabled level to a valid signal level. The voltage present at the output prior to the enabling of the output can significantly affect the measurement. To provide the most useful measurements, the starting voltages will reflect those in realistic applications. The capacitive load used for testing is not specified in this standard, due to the widely varying nature of applications, but should be specified in all data sheets.

In differential applications, it is assumed that the device has been terminated with a characteristic load across the outputs. This would cause the differential outputs to collapse together when disabled. To measure enable times, the parameter is measured from the time a valid enable signal is received until the output achieves a valid output voltage differential. For disable times, the parameter is measured from the time a valid disable signal is received, until the output begins to collapse towards the termination voltage.

5.1 Testing single ended output enable and disable times

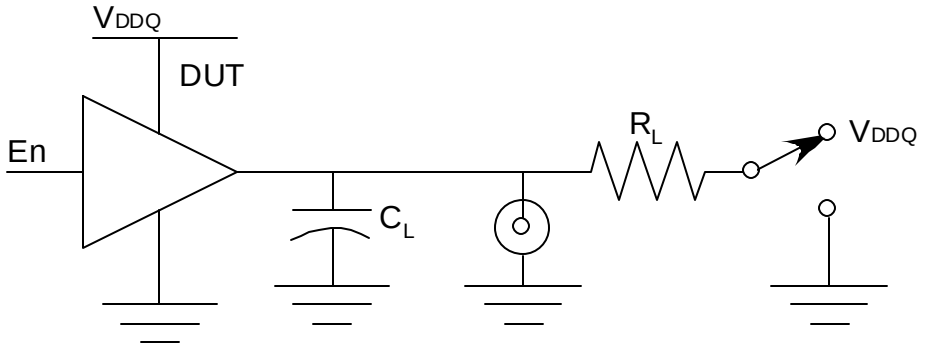


Figure 7 — Testing configuration for single ended output enable and disable times.

5 Test circuits and waveforms (cont'd)

5.1 Testing single ended output enable and disable times (cont'd)

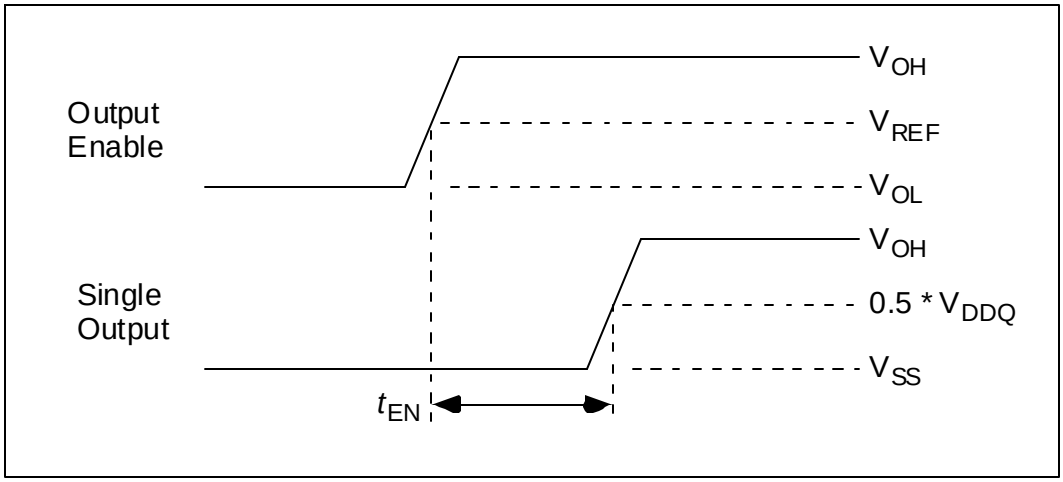
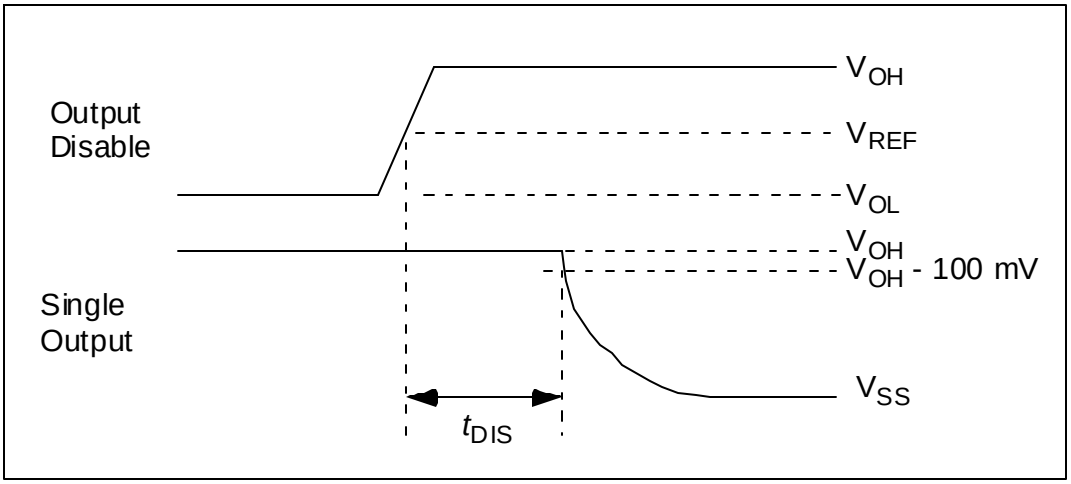


Figure 8 — Single ended enable time measurements



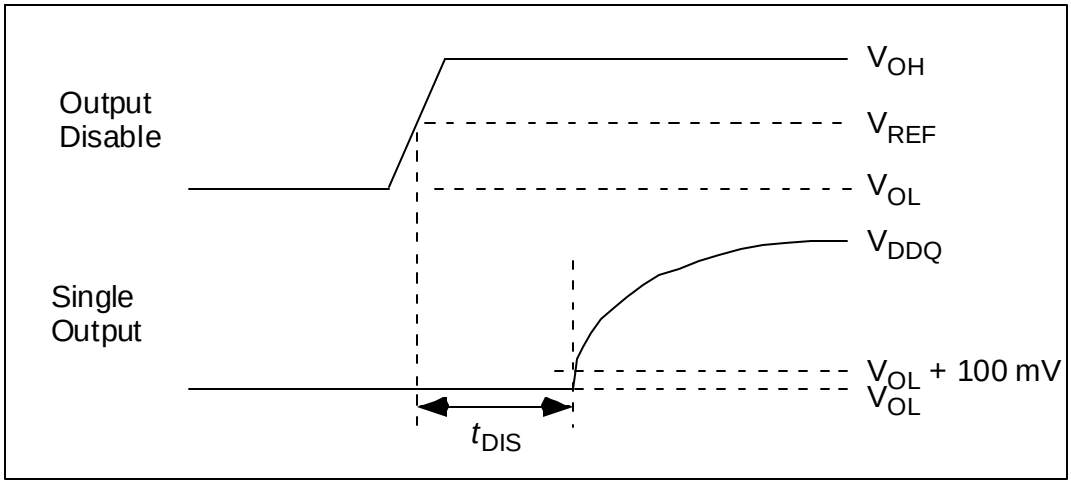


Figure 9 — Single ended disable time measurements

5 Test circuits and waveforms (cont'd)

5.2 Testing differential output enable and disable times

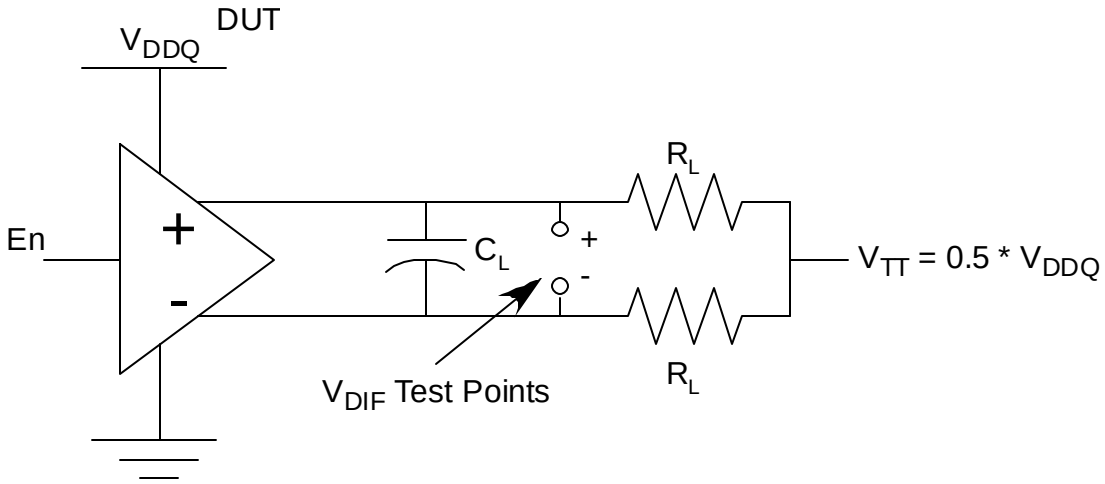


Figure 10 — Testing configuration for output enable and disable times on differential outputs.

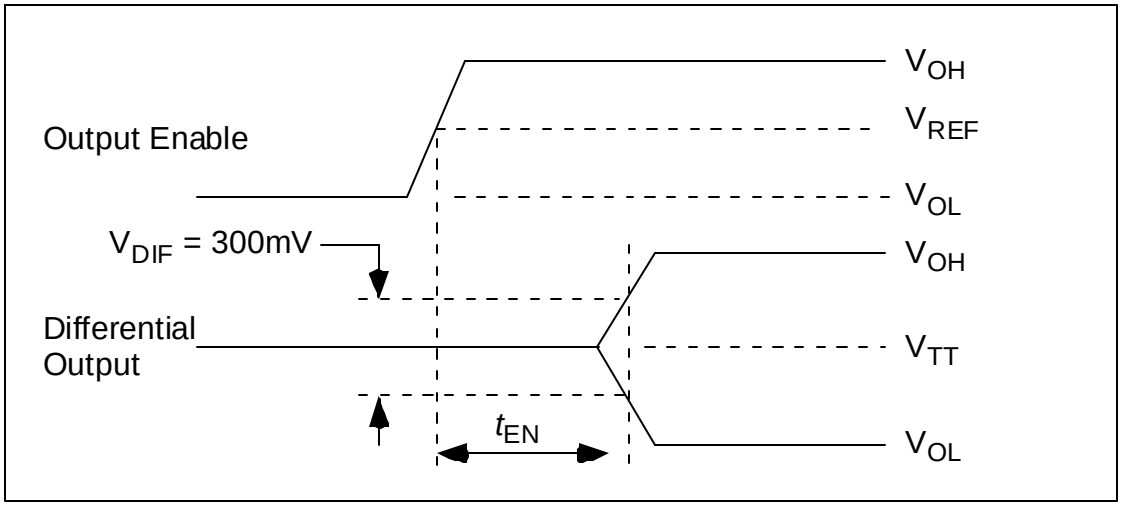


Figure 11 — Differential enable time measurements

5 Test circuits and waveforms (cont'd)

5.2 Testing differential output enable and disable times (cont'd)

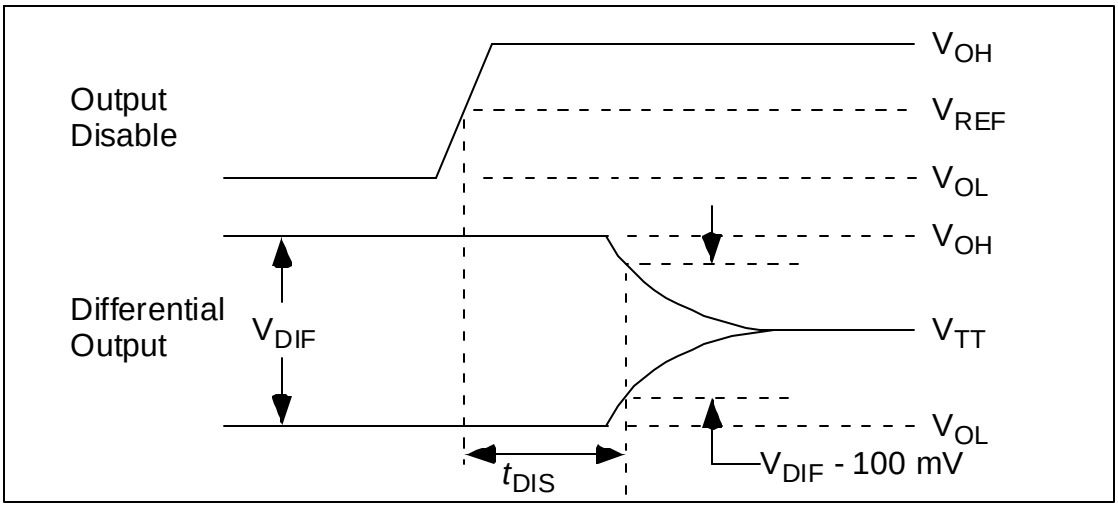


Figure 12 — Differential disable time measurements

6 Use of the BIC name

The BIC standard contains several variations on the interface, including single ended, differential, drive strengths, and the possible use of On Die Termination. The standard has been designed so that all devices that utilize the single ended version of BIC should be capable of inter-device communications (at a modest data rate) over a BIC interface, regardless of class type. All differential BIC devices should be capable of communicating over a differential BIC interface (at modest performance). The output classes and ODT allow focusing the interface characteristics to optimize performance under defined conditions.

There are other applications, beyond those described in the standard that may need a BIC interface with slightly different characteristics.

For a single ended interface to claim compliance to the BIC standard, compliance with the following sections (and associated subsections) is mandatory:

1) 3.1 – Supply Voltage Levels
2) 3.2 – Input Voltage Levels
3) 3.4 – Output Characteristics

For a single ended BIC interface, compliance with the following sections is optional:

1) 3.3 – Devices with On Die Termination (ODT)
2) 3.5 – BIC Output Classes
3) 3.6 – Termination information for all classes (for reference only)

For a differential interface to claim compliance to the BIC standard, compliance with the following sections (and associated subsections) is mandatory:

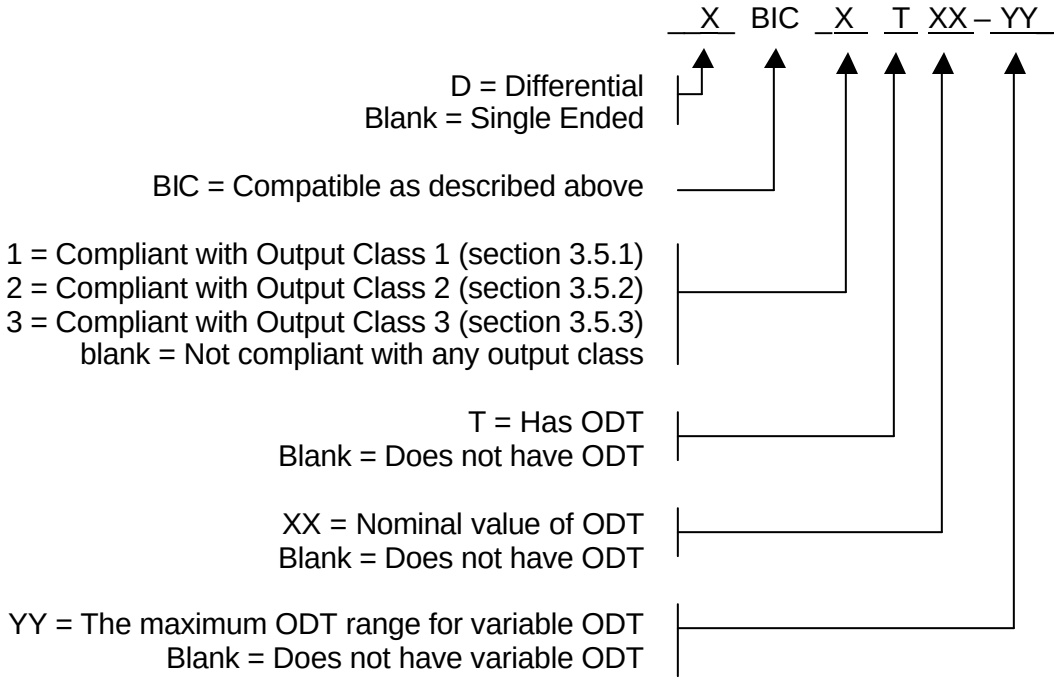
1) 4.1 – Supply Voltage Levels
2) 4.2 – Input Voltage Levels
3) 4.3 – Output Characteristics

For a differential BIC interface, compliance with the following sections is optional:

1) 4.4 – Applications information for differential BIC interfaces (for reference only)

6 Use of the BIC name (cont'd)

It is possible to fully describe a BIC interface through the name. The guidelines as follows:



As an example, a single ended device with class-1 output drivers and 50 ohm ODT could be described as BIC1T50. A single ended device with class-3 output drivers and no ODT could be described as BIC3.

7 Reference to other applicable JEDEC standards and publications

JEDEC Standard JESD8-6, *High Speed Transceiver Logic (HSTL)*. A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits. BIC Class 1 is comparable to HSTL Class 1, but operating from a nominal V_{DDQ} of 1.2 V as described in Section 3.1 above. BIC Class 2 can similarly be compared with HSTL Class 2. BIC Class 3 has no equivalent comparison with any existing HSTL class.

Annex A (informative) Differences between JESD8-16A and JESD8-16

This table briefly describes most of the changes made to entries that appear in this standard, JESD8-16A, compared to its predecessor, JESD8-16 (April 2004). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Description of change

General changes: Titles were added to all of the tables.

Section 1: New wording to reflect the new structure of the document.

Section 2: No changes

Section 3.1: No specification changes. Note 3 has been altered.

Section 3.2: No specification changes.

Section 3.3 and subsections: Entirely new.

Section 3.4 and subsections: Table 7 and the associated notes are unchanged from the released spec. All other material is in new.

Section 3.5 and subsections: Document structure has changed. This was formerly part of the previous section. Contains significant format changes from the released standard.

Section 4: Unchanged

Section 5: Figure 4 changed to reflect industry standard timing point. No other changes.

Section 6: Entirely new.

Standard Improvement Form **JEDEC JESD8-16A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
2500 Wilson Blvd. Suite 220
Arlington, VA 22201-3834
Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC